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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,999	06/20/2003	William H. Robertson	CA7010223001	5787
23639	7590	01/11/2006	EXAMINER	
BINGHAM, MCCUTCHEN LLP THREE EMBARCADERO CENTER 18 FLOOR SAN FRANCISCO, CA 94111-4067			WHITMORE, STACY	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/600,999

Applicant(s)

ROBERTSON ET AL.

Examiner

Stacy A. Whitmore

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 54-88 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 54-88 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/1/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 54-88 are rejected under 35 U.S.C. 102(b) as being anticipated by Dieckman, D., "DISCOE: distributed design and analysis to preserve intellectual property".
2. As for the claims 54-88, Dieckman discloses the invention as claimed, including:
3. A method (computer program product and system comprising means for) of providing remotely located circuit design resources, the method comprising:
connecting a plurality of user nodes to a portal over a distributed electronic network [pg. 58, section II, fig. 1 – showing user nodes to a distributed network which comprises portal for a connection];
connecting a plurality of supplier nodes to the portal over the distributed electronic network [pg. 58, section II, fig. 1 – showing supplier nodes to a distributed network which comprises portal for a connection];
making available a plurality of circuit design resources through the portal, at least one of the plurality of circuit design resources being located in one of the plurality of user and supplier nodes [pg. 58, section II, fig. 1 – showing user and supplier nodes to a distributed network which comprises portal for a connection and resources located at both the user and supplier nodes];

receiving one or more requests from at least one of the plurality of user nodes for access to one or more of the plurality of circuit design resources available through the portal and not located on the at least one user node [pg. 58, section II, fig. 1 – showing user and supplier nodes to a distributed network which comprises portal for a connection and resources located at both the user and supplier nodes, and pg. 59, Front-end design framework section showing users interact with and make requests for access to resources]; and

automatically responding to the one or more requests from the at least one user node [pg. 58, section II, fig. 1 – showing user and supplier nodes to a distributed network which comprises portal for a connection and resources located at both the user and supplier nodes, and pg. 59, Front-end design framework section showing users interact with and make requests for access to resources and shows the suppliers automatically respond].

wherein the plurality of circuit design resources comprise component data, the component data being stored in one or more databases located on the portal and/or on one or more of the plurality of user and supplier nodes [pg. 58, section II, fig. 1 – showing user and supplier nodes to a distributed network which comprises portal for a connection and resources located at both the user and supplier nodes, and pg. 59, Front-end design framework section showing users interact with and make requests for access to resources and shows the suppliers automatically respond, also showing component data].

wherein the component data comprises component data sheets, timing models, application notes, simulation models, and/or signal integrity models [pg. 58, section II, fig. 1 – showing user and supplier nodes to a distributed network which comprises portal for a connection and resources located at both the user and supplier nodes, and pg. 59-60, Front-end design framework section showing users interact with and make requests for access to resources and shows the suppliers automatically respond, also showing data sheets, timing models (included in simulation for verification), application notes (information sharing), simulation models, and/or signal integrity models (also included in simulation and verification)].

wherein the plurality of circuit design resources comprise a plurality of virtual circuit blocks, each of the plurality of virtual component blocks being stored in one or more databases located on the portal and/or on one or more of the plurality of user and supplier nodes [pg. 58, IP contained in vendor libraries, pg. 59, intellectual property reuse, and intellectual property distribution].

wherein the plurality of circuit design resources comprise a plurality of electronic design automation tools [pg. 57, right hand side shows design activities being collaborative and design integration, pg. 58, section II, especially right hand side, "The ability to construct....multi-organizational design activities...", pg. 59, design capture, simulation verification, modeling].

wherein the plurality of circuit design resources comprise a listing of suppliers of integrated circuit fabrication services [pg. 58, section II showing multiple vendors, libraries, pg. 59, left hand side showing multiple catalogs, placing information online for use, access to design entities].

wherein the plurality of circuit design resources comprise information on expert design services [pg. 59, parts catalogs, structural and functional specifications, information sharing, IP are forms of expert design services].

wherein automatically responding to the one or more requests from the at least one user node comprises:

determining whether each of the one or more requested circuit design resources are located on the portal; acquiring each of the one or more requested circuit design resources not located on the portal from one or more of the plurality of user and supplier nodes; and transmitting the one or more requested circuit design resources to the at least one user node [pg. 58, fig. 1, pg. 60, Distributed simulation/IP preservation section showing that resources are found, acquired, and transmitted to at least one user node].

wherein automatically responding to the one or more requests from the at least one user node comprises:

determining whether each of the one or more requested circuit design resources are located on the portal; and providing information to the at least one user node on how to access each of the one or more requested circuit design resources not located on the

portal [pg. 58, fig. 1, pg. 60, Distributed simulation/IP preservation section showing that resources are found, acquired, and transmitted to at least one user node, pg. 59, Version Control showing information on how to access design resources].

wherein the information provided to the at least one user node comprises linking information to one or more of the plurality of user and supplier nodes where the one or more requested circuit design resources are located [pg. 58, figure 1 shows linking information].

wherein automatically responding to the one or more requests from the at least one user node comprises:

determining whether each of the one or more requested circuit design resources are located on the portal; and sending information to the at least one user node on how to obtain each of the one or more requested circuit design resources not located on the portal [pg. 58, fig. 1, pg. 60, Distributed simulation/IP preservation section showing that resources are found, acquired, and transmitted to at least one user node, pg. 59, Version Control showing information on how to access design resources].

wherein the information sent to the at least one user node comprises a username and password [pg. 60, user authentication].

wherein automatically responding to the one or more requests from the at least one user node comprises:

determining whether each of the one or more requests from the at least one user node can be fulfilled at the portal; and forwarding each of the one or more requests that cannot be fulfilled at the portal to one or more of the plurality of user and supplier nodes [pg. 58, fig. 1, pg. 60, Distributed simulation/IP preservation section showing that resources are found, acquired, and transmitted to at least one user node,].

maintaining prior usage information relating to the one or more requests received from the at least one user node at the portal [pg. 59, Version Control information].

maintaining profile data on each of the plurality of user and supplier nodes at the portal [pg. 59, Version Control information].

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4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW

January 6, 2006

A handwritten signature in black ink, appearing to read 'SAW', is located below the typed name of the examiner.